PACKAGED MICROELECTRONIC DEVICES WITH INTERCONNECTING UNITS AND METHODS FOR MANUFACTURING AND USING THE INTERCONNECTING UNITS

TECHNICAL FIELD

The present invention relates to packaging microelectronic devices having a microelectronic die including an integrated circuit. More particularly, several aspects of the invention are related to an interconnecting unit for operatively coupling the microelectronic die to voltage sources, signal sources, and other input/output sources.

BACKGROUND

Microelectronic devices, such as memory devices and microprocessors, typically include a microelectronic die encased in a protective covering. The die can include memory cells, processor circuits, interconnecting circuitry and/or other functional features. The die also typically includes an array of very small bond-pads electrically coupled to the functional features. When the die is packaged, the bond-pads are coupled to leads, solder ball-pads or other types of terminals for operatively coupling the microelectronic dies to buses, circuits and/or other microelectronic devices.

Several different techniques have been developed for packaging microelectronic dies. The dies, for example, can be incorporated into individual packages, mounted with other components in hybrid or multiple chip modules, or connected directly to a printed circuit board or other types of substrates. When a die is incorporated into an individual package, the bond-pads on the die are typically coupled to a lead frame, and the die is covered or otherwise sealed from the environment. When the die is attached directly to a printed circuit board or another type of substrate, the bond-pads on the die are typically coupled to corresponding contact elements on the substrate using wire-bond lines, ball grid arrays and other techniques. The dies that are mounted directly to the substrates are generally Chip Scale Package devices (CSP) or Flip Chip Bare Die devices (Flip-Chip).

CSP and Flip-Chip devices generally have one or more protective casings that encapsulate the dies and any exposed contact elements, bond-pads or wire-bond lines. The protective casings should shield the die and the other components on the substrate from environmental factors (*e.g.*, moisture), electrical interference, and mechanical shocks. The protective casings are accordingly robust elements that protect the sensitive components of a microelectronic device. The protective casings are generally composed of plastics, ceramics, or thermosetting materials.

One conventional technique for fabricating the protective casings involves placing the die in a cavity of a mold, and then injecting a thermosetting material into the cavity. The thermosetting material flows over the die on one side of the substrate until it fills the cavity, and then the thermosetting material is cured so that it hardens into a suitable protective casing for protecting the die. The protective casing should not have any voids over the die because contaminants from the molding process or environmental factors outside of the mold could damage the die. The thermosetting material, moreover, should not cover a ball-pad array on the substrate or damage any electrical connections between the die and the substrate. Therefore, the thermosetting material should be molded in a manner that avoids (a) producing voids in the protective casing, (b) covering certain portions of the substrate, and (c) displacing or otherwise damaging any wire-bond lines or solder joints between the die and the substrate.

One drawback of forming protective casings is that the thermosetting material may leak between the substrate and a mold assembly as the thermosetting material fills the mold. The thermosetting material generally leaks because the substrates can have small surface asperities and/or be warped. Such leaking of the thermosetting material can cover ball-pad arrays and/or adhere to the mold. When the thermosetting material covers a portion of the ball-pad array, the packaged device is typically rejected because it cannot be electrically coupled to a module. Additionally, the molds must be cleaned periodically to remove the thermosetting material that adheres to the mold. Cleaning the molds, however, is difficult because they operate at approximately 180°C, and thus they are difficult to handle and they must also be reheated after they have been cleaned. The down time for cleaning a mold can be approximately 15% of the available operating time for a molding machine.

Therefore, it would be desirable to prevent the thermosetting material from leaking between the substrate and the mold.

One technique that addresses the leakage between the substrate and the mold is to cover the inside of the mold with a thin plastic film. This technique, however, is time consuming because the mold must generally be cooled to a temperature at which it can be handled, and it is difficult to attach the plastic film to the mold without creating wrinkles in the plastic film. Moreover, if the plastic film has wrinkles, the resulting protective casings may have surface asperities that are either unsightly or impair the performance of the protective casing. Therefore, covering the inside of a mold with a thin plastic film is not a good solution for preventing the thermosetting material from leaking between the substrate and the mold.

SUMMARY

The present invention is directed toward methods and apparatuses for encapsulating a microelectronic die or other components in the fabrication of packaged microelectronic devices. In one aspect of the invention, a packaged microelectronic device assembly includes a microelectronic die, a substrate attached to the die, a protective casing covering a portion of the substrate, and a barrier projecting away from the surface of the substrate. The microelectronic die can have an integrated circuit and a plurality of bond-pads operatively coupled to the integrated circuit. The substrate can have a cap-zone defined by the area covered by the protective casing, a plurality of contact elements arranged in the cap-zone, a plurality of ball-pads arranged in a ball-pad array outside of the cap-zone, and a plurality of conductive lines coupling the contact elements to corresponding ball-pads. The barrier is configured so that at least a portion of the barrier is outside of the cap-zone and adjacent to at least a portion of the molded section. The barrier, for example, can be a thin tape applied to the substrate, a polymeric coating covering the substrate, another type of thin film disposed on the substrate, or a ridge formed from the substrate itself. The barrier can have an opening with an edge that borders the cap-zone so that the area of the cap-zone is not covered by the barrier. In operation, the barrier inhibits the thermosetting material from covering a portion of the substrate outside of the cap-zone. As such, the barrier prevents or

at least inhibits the thermosetting material from leaking between the substrate and a mold outside of the cap-zone during a molding process.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A is top cut-away isometric view of a microelectronic device before being packaged in accordance with one embodiment of the invention.

Figure 1B is a bottom isometric view of the microelectronic device of Figure 1A.

Figure 2A is a side cross-sectional view of the microelectronic device of Figure 1A being packaged in accordance with an embodiment of the invention.

Figure 2B is a front cross-sectional view of the microelectronic device of Figure 2A being packaged in accordance with an embodiment of the invention.

Figure 3 is a top isometric view of a packaged microelectronic device in accordance with an embodiment of the invention.

Figure 4 is a top isometric view of a microelectronic device before being packaged in accordance with another embodiment of the invention.

Figure 5A is a top isometric view of a packaged microelectronic device in accordance with another embodiment of the invention.

Figure 5B is a bottom isometric view of the packaged microelectronic device of Figure 5A.

Figure 6 is a top isometric view of a microelectronic device before being packaged in accordance with yet another embodiment of the invention.

DETAILED DESCRIPTION

The following disclosure is directed toward packaged microelectronic devices, interconnecting units for packaged microelectronic devices, and methods for encapsulating a microelectronic die, wire-bond lines or other components of a microelectronic device. Several embodiments of the invention are described with respect to memory devices, but the methods and apparatuses are also applicable to microprocessors and other types of devices. One skilled in the art will accordingly understand that the present invention may have

additional embodiments, or that the invention may be practiced without several of the details described below.

Figure 1A is a top cutaway isometric view of a microelectronic device 10 in accordance with one embodiment of the invention before it has been encapsulated. The microelectronic device 10 can include a substrate 20 and a microelectronic die 40 attached to the substrate 20 by an adhesive 60. The microelectronic device 10 shown in Figure 1 illustrates the substrate 20 and the die 40 before forming protective casings that encapsulate the die 40 and portions of the substrate 20. The following description is directed toward encapsulating a microelectronic die on a flexible substrate, but it is expected that several embodiments of methods and apparatuses in accordance with the present invention may be used to encapsulate a large variety of electrical and/or non-electrical articles. Therefore, the following description with respect to encapsulating the microelectronic die 20 shown in Figures 1A-6 is for the purpose of illustration only and it is not intended to limit the scope of the invention.

The embodiment of the substrate 20 shown in Figure 1A can have a first end 21, a second end 22 opposite the first end 21, a first surface 23, and a second surface 24 opposite the first surface 23. The substrate 20 can also include an elongated slot 25 between the first and second surfaces 23 and 24 that extends lengthwise along a medial portion of the substrate 20. Additionally, an aperture 26 through the substrate 20 can be located at a secondary gate location that is generally proximate to the second end 22 of the substrate 20. The substrate 20 is one component of an interconnecting unit that provides a plurality of interconnects, such as an array of ball-pads, for coupling very small bond-pads on the microelectronic die 40 to voltage sources, signal sources, and/or other input and output sources. The interconnects can be electrical components or optical components that transmit a signal. In the embodiment shown in Figure 1A, the substrate 20 includes a plurality of interconnects defined by an array of ball-pads 27, an array of contact elements 28 proximate to the slot 25, and a trace 29 or other type of conductive line between each ball-pad 27 and a corresponding contact element 28. The substrate 20 can be a flexible material or a substantially rigid material, and the traces 29 can be conductive lines that are printed on the substrate in a manner similar to printed circuit boards.

The embodiment of the microelectronic die 40 shown in Figure 1A includes a first side 41 attached to the second surface 24 of the substrate 20 by the adhesive 60. The microelectronic die 40 can also include a plurality of small bond-pads 42 and an integrated circuit 44 (shown schematically) coupled to the bond-pads 42. The bond-pads 42 are arranged in an array along the first side 41 of the microelectronic die 40 so that the bond-pads 42 are aligned with or otherwise accessible through the slot 25 in the substrate 20. A plurality of wire-bond lines 50 or other types of connectors couple the bond-pads 42 on the die 40 to corresponding contact elements 28 on the substrate 20. As such, the substrate 20 distributes the very small bond-pads 42 to the larger array of ball-pads 27. Referring to Figure 1B, the die 40 can project away from the second surface 24 of the substrate 20.

Referring again to Figure 1A, the contact elements 28, the bond-pads 42, and the connectors 50 are arranged in a cap-zone defined by an area that is to be encapsulated by a protective casing. In the embodiment shown in Figure 1A, the microelectronic device 10 has a first cap-zone over the first surface 23 of the substrate 20 shown by an area A x B. The cap-zone can have a different configuration for a different type of microelectronic device. In other embodiments, for example, the cap-zone can be around the die 40 over the second surface 24 of the substrate.

The microelectronic device 10 shown in Figure 1A can also include a barrier 30 disposed on the substrate 20. The barrier 30 is another component of the inter-connecting unit along with the substrate 20. In this embodiment, the barrier 30 has an opening 32 surrounding the cap-zone A x B on the substrate 20. The opening 32 in the barrier 30 can be adjacent to the border of the cap-zone A x B to completely surround the cap-zone A x B. The barrier 30 can accordingly cover the ball-pads 27 on the substrate, but the contact elements 28, the bond-pads 42, and the wire-bond lines 50 are exposed through the opening 32 of the barrier 30. In other applications, only a portion of the barrier 30 is adjacent to only a portion of the cap-zone. The barrier 30, for example, could be adjacent to the elongated sides of the cap-zone along the contact elements 28 and the end of the cap-zone at the aperture 26, but the barrier 30 may not cover the area at the first end 21 of the first surface 23 of the substrate 20. The barrier 30 is accordingly disposed on the substrate 20 outside of the cap-zone A x B so that at least a portion of the barrier 30 is adjacent to at least a portion of the cap-zone A x B. As explained in more detail below, the barrier 30 acts as a gasket that

inhibits or prevents a thermosetting material from leaking outside of the cap-zone between the substrate 20 and a mold assembly.

The barrier 30 is applied to or otherwise formed on the substrate 20 before molding a protective casing over the cap-zone. In the embodiment shown in Figure 1A, the barrier 30 is a thin film, such as a tape, that is adhered to the substrate 20, or a pliable polymeric coating that is deposited onto the substrate 20. The barrier 30 can alternatively be made from other materials. In one embodiment, the barrier 30 is a roll of tape having a plurality of apertures that is applied to a continuous strip of substrate material having a plurality of slots so that each opening of the tape surrounds a corresponding slot. The strip can be cut to form a separate interconnecting unit having one or more individual pairs of the substrate 20 and the barrier 30. In another embodiment, the barrier 30 is an individual piece of tape applied to an individual substrate 20. In still another embodiment, the barrier 30 is a coating of a polymeric material, rubber, or other compressible and/or pliable material that is deposited onto the substrate 20. Such coatings can be deposited by screen printing techniques, or by spraying a layer of material on the substrate.

Figures 2A and 2B illustrate an embodiment of a method for encapsulating the microelectronic device 10 using a mold assembly having a first mold section 200 and a second mold section 300. The first mold section 200 has a bearing surface 220 and a wire-side cavity 224, and the second mold section 300 has a bearing surface 320 and a die-side cavity 324. The wire-side cavity 224 is configured to form a first protective casing over the cap-zone A x B shown in Figure 1A, and the die-side cavity 324 is configured to form a second protective casing over the die 40 shown in Figure 1B. The second mold section 300 can also include a gate 326 and an injection chamber 328 through which a flow "*F*" of mold compound (*e.g.*, thermosetting material) is injected into the die-side cavity 324.

During the molding process, the microelectronic device 10 is positioned in the mold assembly to align the die 40 with the die-side cavity 324 and to align the cap-zone A x B with the wire-side cavity 224 (best shown in Figure 2B). In this embodiment, the bearing surface 220 of the first mold section 200 presses against a perimeter portion 34 of the barrier 30, and the bearing surface 320 of the second mold section 300 presses against the second surface 24 of the substrate 20. The bearing surface 220 of the first mold section 200 can press against the perimeter portion 34 of the barrier 30 by injecting a mold compound

into the die-side cavity 324, as explained in U.S. Patent Application No. 09/255,554, which is herein incorporated by reference. The flow of mold compound *F* initially passes through the gate 326 of the second mold section 300. The flow of mold compound *F* continues into the die-side cavity 324 to create a first flow A_1 heading in a first direction toward the second end 22 of the substrate 20. The first flow of mold compound A_1 passes through the aperture 26 in the substrate 20 to generate a second flow of mold compound B_1 that flows through the wire-side cavity 224 of the first mold section 200. The second flow of mold compound B_1 fills the slot 25 of the substrate 20 and flows in a second direction until it reaches a terminal end 227 of the wire-side cavity 224.

The barrier 30 on the substrate 20 is expected to inhibit or prevent the mold compound from leaking between the first side 23 of the substrate 20 and the bearing surface 220 of the first mold section 200. For example, as the pressure of the mold compound builds in the die-side cavity 324, the pressurized mold compound drives the substrate 20 toward the first mold section 200 to press the perimeter portion 34 of the barrier 30 against the bearing surface 220. The perimeter portion 34 of the barrier 30 accordingly fills small voids or surface asperities on both the first surface 23 of the substrate 20 and the bearing surface 220 of the first mold section 200. As such, the perimeter portion 34 of the barrier 30 inhibits the mold compound from leaking at the second end 22 of the substrate 20. Moreover, as shown by Figure 2B, the barrier 30 also inhibits or prevents the mold compound from leaking between the substrate 20 and the bearing surface 220 of the first mold section 200 in a lateral direction *L* relative to the second flow of mold compound B_1 (Figure 2A). The barrier 30 accordingly prevents the mold compound from inadvertently covering the ball-pads 27 on the first surface 23 of the substrate 20 or fouling the mold assembly at the second end 22 of the substrate 20.

One expected advantage of the embodiment of the barrier 30 shown in Figures 1A-2B is that it is expected to reduce or prevent the mold compound from leaking between the substrate 20 and the first mold section 200. The bearing surface 220 of the first mold section 200 is thus less likely to be fouled by the mold compound, and the ball-pads 27 are also less likely to be covered by mold compound. As a result, the embodiment of the microelectronic device 10 with the barrier 30 shown above in Figures 1A-2B is expected to reduce the downtime for cleaning the mold assembly and the number of rejected parts.

Figure 3 illustrates the microelectronic device 10 after a first protective casing 72 has been formed over the cap-zone A x B. The barrier 30 can remain on the substrate 20 in subsequent processing steps, such as reflow processing, marking, and other post-encapsulation processes. The barrier 30 can accordingly protect the ball-pads 27 until solder balls are deposited onto corresponding ball-pad 27. As such, another expected advantage of the microelectronic device 10 is that the barrier 30 can protect the substrate 20 from being damaged in other processes after fabricating the casings 72 and 74.

Figure 4 is a top isometric view of a microelectronic device 410 in accordance with another embodiment of the invention. In this embodiment, the microelectronic device 410 includes the substrate 20 and the die 40. The substrate 20 and the die 40 can be similar to the components described above with reference to Figures 1A-2B, and thus like reference numbers refer to like components in Figures 1A-4. The microelectronic device 410 can also include a barrier 430 having an opening 432 and a plurality of apertures 436. The opening 432 exposes the cap-zone A x B such that at least a portion of the barrier 430 is adjacent to at least a portion of the cap-zone A x B. The apertures 436 are arranged in a pattern corresponding to the pattern of ball-pads 27 on the substrate 20. Each aperture 436 exposes a corresponding ball-pad 27 such that a solder ball or a solder paste pad can be deposited onto the ball-pads 27 without removing the barrier 30. The solder balls can be deposited onto the ball-pads 27 using pen dispensers, and the solder paste pads can be deposited into the apertures 436 of the barrier 430 using screen printing techniques known in the art. In a typical application, a protective casing is formed in the opening 432 of the barrier 430 to cover the slot 25 and the contact elements 28 in a manner similar to the method set forth above with respect to Figures 2A and 2B. After a protective casing is formed over the cap-zone A x B of the substrate 20, the microelectronic device 410 is removed from the mold assembly and the solder balls or solder paste pads can be deposited onto the ball-pads 27.

The embodiment of the microelectronic device 410 shown in Figure 4 is expected to prevent the mold compound from leaking between the substrate 20 and the mold assembly in a manner similar to the microelectronic device 10 described above. The microelectronic device 410 is also expected to enhance the protection of the substrate 20 in subsequent processing steps because the barrier 430 can remain on the substrate 120 throughout a reflow procedure for melting the solder balls or the solder paste pads. After the

reflow procedure, the barrier 430 can be peeled or etched from the substrate 20 to remove the barrier 430 before attaching the microelectronic device 410 to a printed circuit board or other assembly. The barrier 430 also enhances the registration of the solder balls or solder paste pads with the ball-pads 27 by providing guides that prevent the solder from bridging between adjacent ball-pads 27. Therefore, the microelectronic device 410 is expected to enhance the throughput and yield of packaged microelectronic devices.

Figure 5A is a top isometric view and Figure 5B is a bottom isometric view of a microelectronic device 510 in accordance with still another embodiment of the invention. In this embodiment, the microelectronic device 510 has a first barrier 530a disposed on the first surface 23 of the substrate 20 and a second barrier 530b disposed on the second surface 24 of the substrate 20. The first barrier 530a can be substantially similar to the barrier 30 described above with reference to Figure 3. The first barrier 530a can accordingly have an opening 532a around the first protective casing 72 such that the first barrier 530a is outside of a first cap-zone on the first side 23 of the substrate 20. The second barrier 530b can be similar to the first barrier 530a, but the second barrier 530b has a second opening 532b around a second protective casing 74 that encapsulates the die 40 (Figure 1B) on the second surface 24 of the substrate 20. The second barrier 530b is accordingly outside of a second cap-zone defined by the second protective casing 74. As such, at least a portion of the first barrier 530a is adjacent to at least a portion of the first cap-zone defined by the first protective casing 72, and at least a portion of the second barrier 530b is adjacent to at least a portion of the second cap-zone defined by the second protective casing 74.

The first and second barriers 530a and 530b shown in Figures 5A and 5B can define the outline of the perimeter or the entire volume of the first and/or second protective casings 72/74. Referring to Figure 5A, the opening 532a is configured to define the perimeter of the protective casing 72. The barriers can also define the entire volume of the casings by having a thickness equal to the desired thickness of the protective casings. The thickness of a barrier can be set by laminating barriers on top of each other or manufacturing the barriers with the full thickness of the casings. One expected advantage of using the barriers to define the perimeter and thickness of the protective casings is that the casings can be formed using a flat tool (*i.e.*, a mold without a cavity). Such flat tooling is generally not complex and it is much easier to clean compared to molds with cavities.

Figure 6 is a top isometric view of a microelectronic device 610 in accordance with another embodiment of the invention. The microelectronic device 610 includes the substrate 20 and the microelectronic die 40 attached to the substrate 20. The microelectronic device 610 can also include a barrier 630 defined by a rim around the cap-zone A x B. The barrier 630 can be a piece of tape, a pliable seal, or a raised portion of the substrate 20. For example, the barrier 630 can be a ridge molded or embossed onto the substrate 20, or the barrier 630 can be decal or a piece of tape that is attached to the first surface 23 of the substrate 20. The barrier 630 can operate in a manner similar to the barrier 130 described above with reference to Figure 1A. The microelectronic device 610 is accordingly expected to inhibit or otherwise prevent a molding compound from leaking between the substrate 20 and a mold assembly during a molding process for forming a protective casing in the cap-zone.

From the foregoing it will be appreciated that specific embodiments of the invention have been disclosed for purposes of enablement and illustration, but that various modifications may be made without deviating from the spirit and the scope of the invention. Accordingly, the invention is not limited except by the appended claims.